

Φ – 575 Διάλεξη 13

Φυσική διατάξεων δισδιάστατων ημιαγωγών

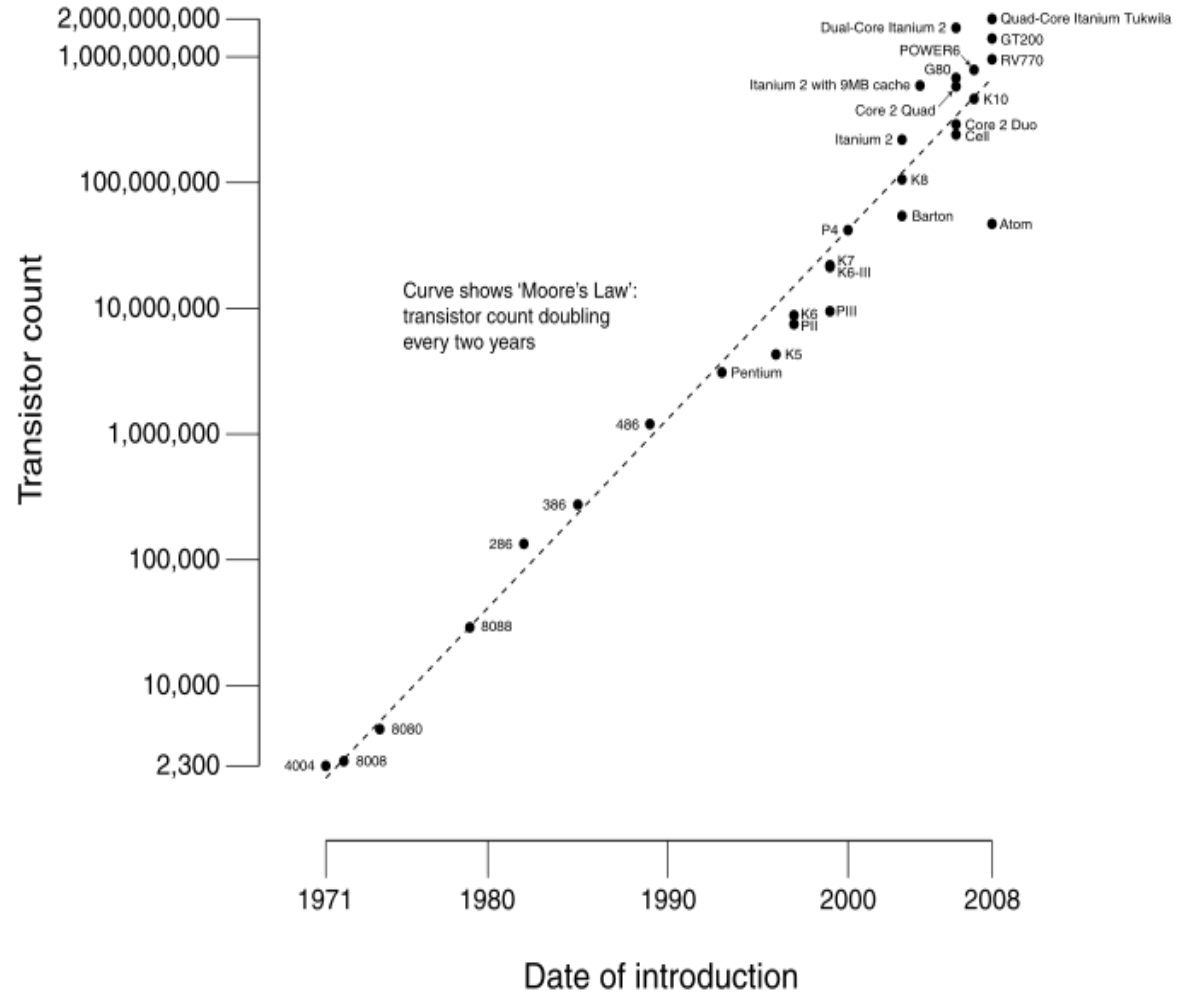
Γιώργος Δεληγεώργης (deligeo@physics.uoc.gr)

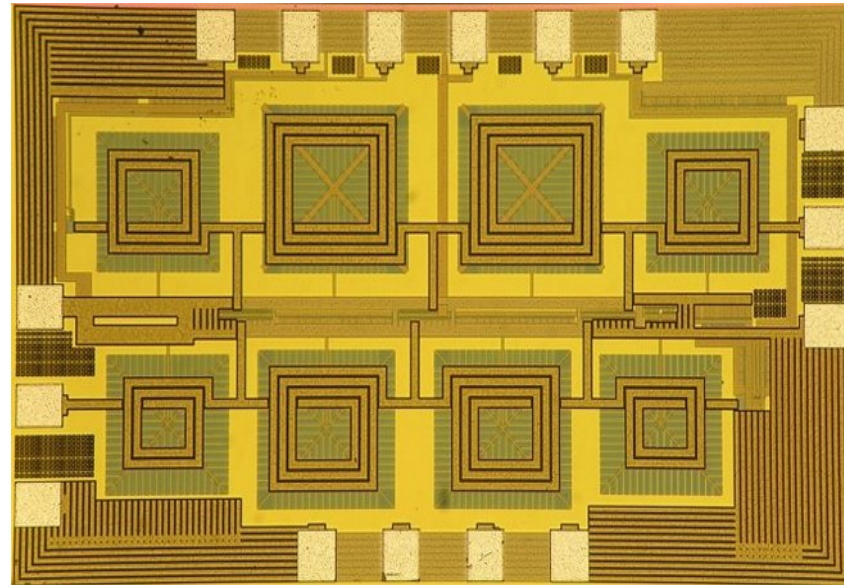
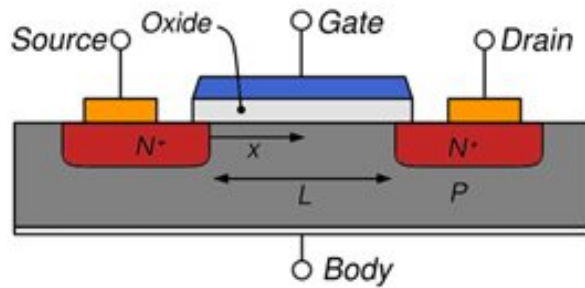


Transistor number:

- Radical increase
- Complex functions
- High operating speed
- Reduced consumption

CPU Transistor Counts 1971-2008 & Moore's Law





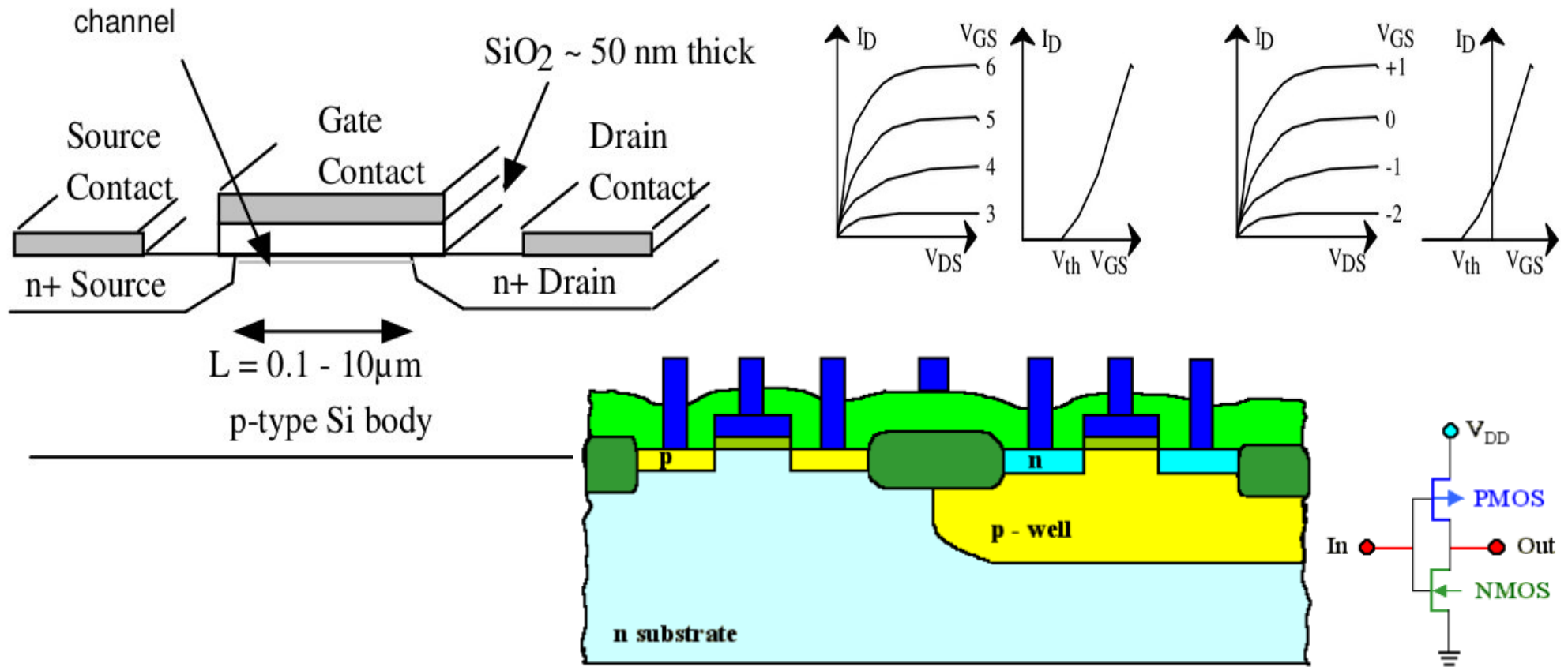
Building blocks:

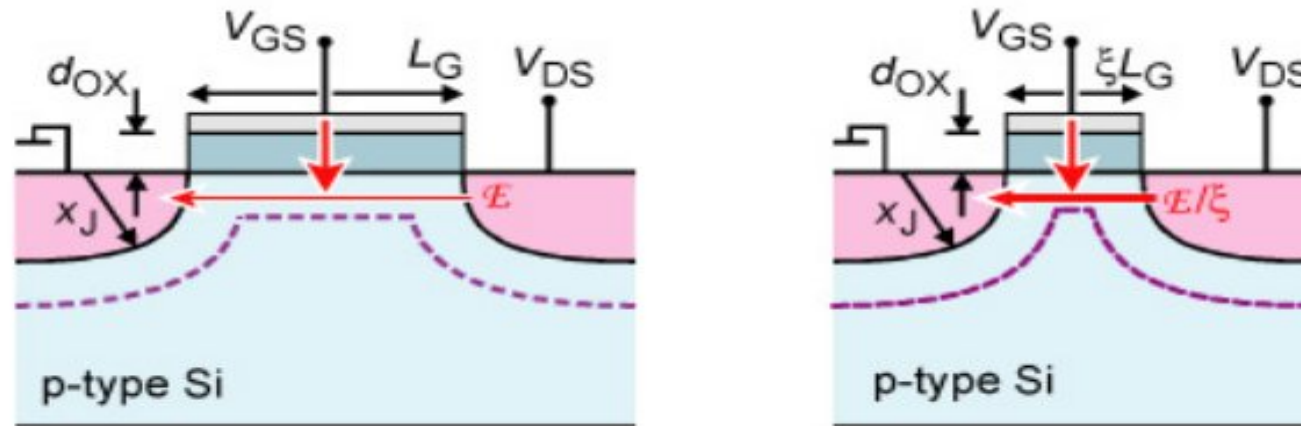
- *Capacitors*
- *Inductances*
- *Resistances*
- *Transistors*
- *Wires*

Fabrication on a flat surface with reduced size

MOSFET:

- Easy construction (planar)
- Small size
- Complementary MOS (CMOS)
- The basis of contemporary electronics

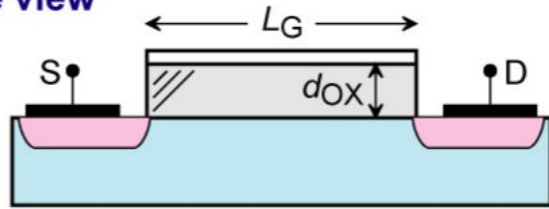




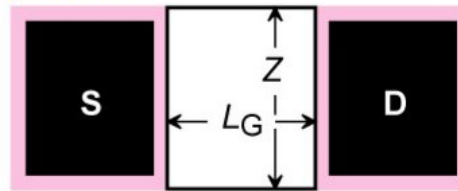
Size reduction:

- *Small footprint thus dense circuits*
- *Small transit time thus faster*
- *Small gate thus reduced paracitic capacitance*
- *Reduced operating voltage thus reduced consumption*

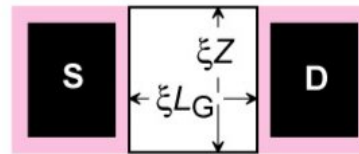
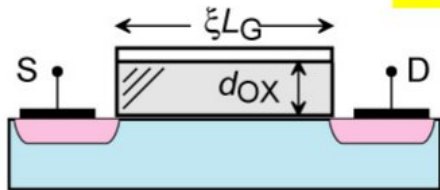
Side view



Top view



Scaling factor ξ

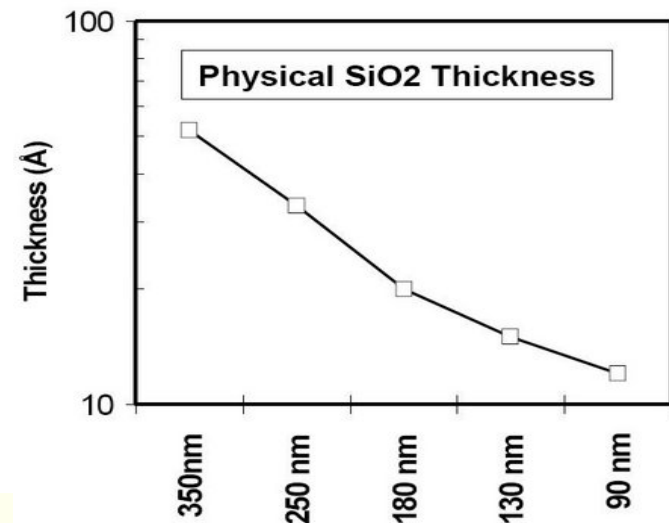


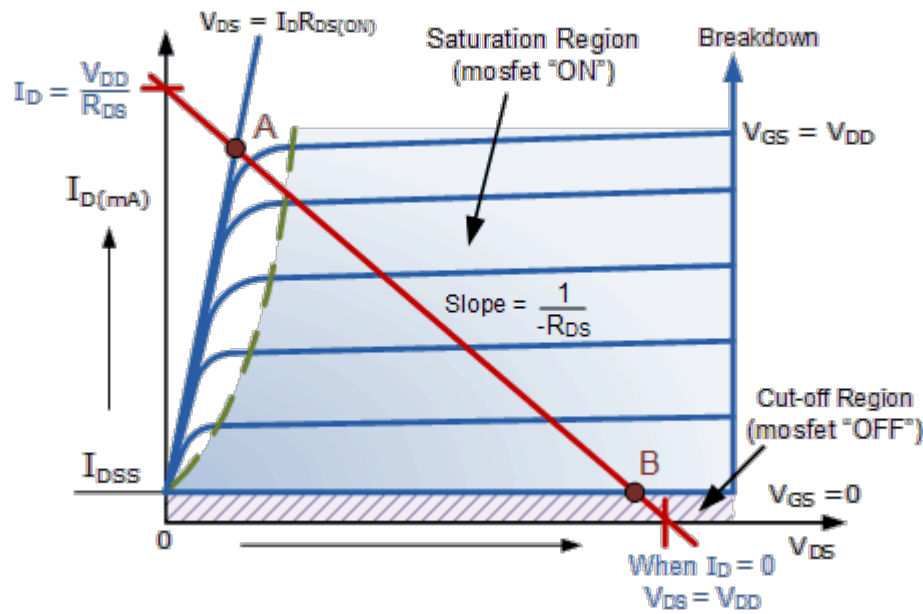
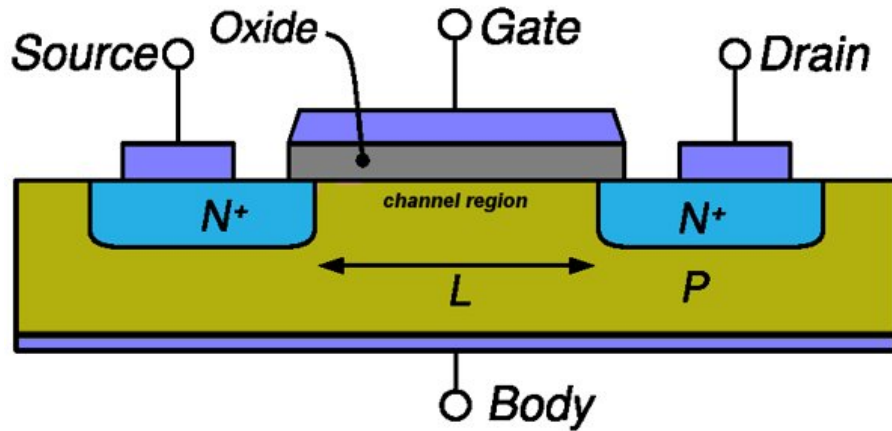
Downscaling by a factor of ξ :

- Size reduction ξ^2
- Gate capacitance $1/\xi^2$
- Operating voltage $1/\xi$
- Speed $\sim \xi$
- Threshold voltage **UNCHANGED**
- Heat density ???

To keep the threshold voltage

- Thinner gate oxide
- Increase in doping density



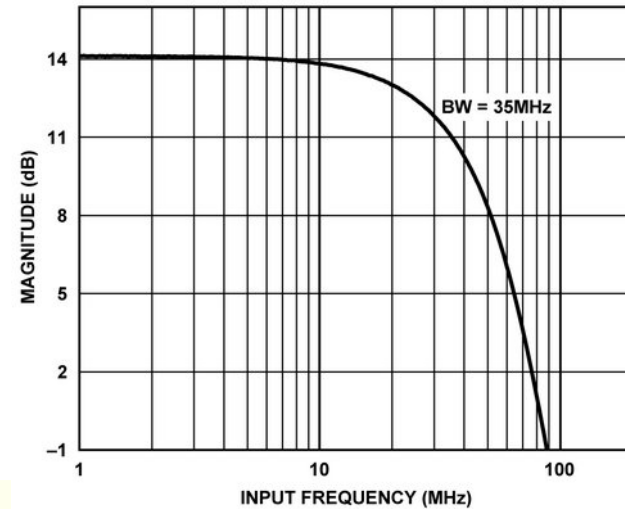


Speed parameters:

- Carrier velocity
 $2 \times 10^7 \text{ cm/s}$
- Channel length

Current control:

- Bandgap
- Access resistance
- Gate - Oxide - Channel capacitor



Instead of reducing the thickness we increase ϵ

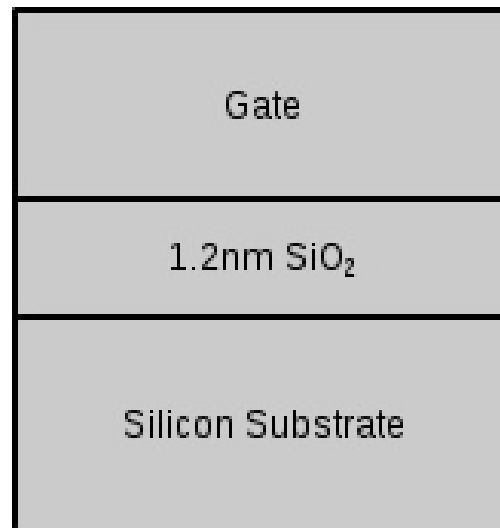
$$C = \frac{\epsilon_o \cdot \epsilon_r \cdot A}{d}$$

Instead of SiO₂ $\epsilon = 3.9$

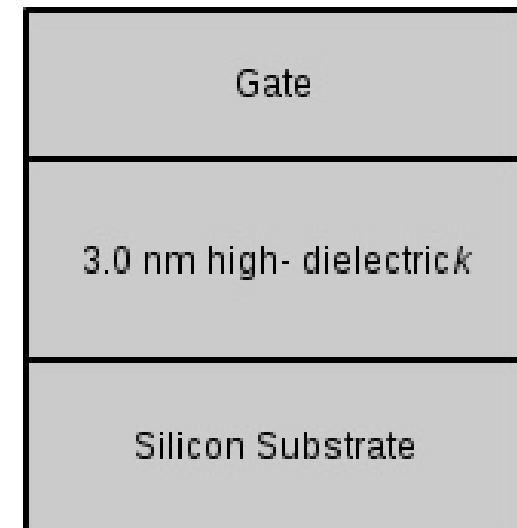
We now use:

HfO $\epsilon = 25$

ZrO₂ $\epsilon = 22$



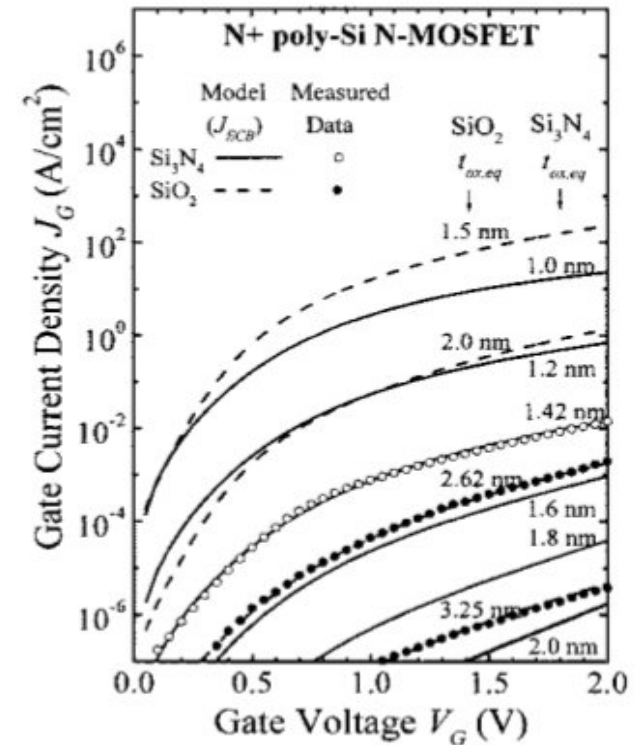
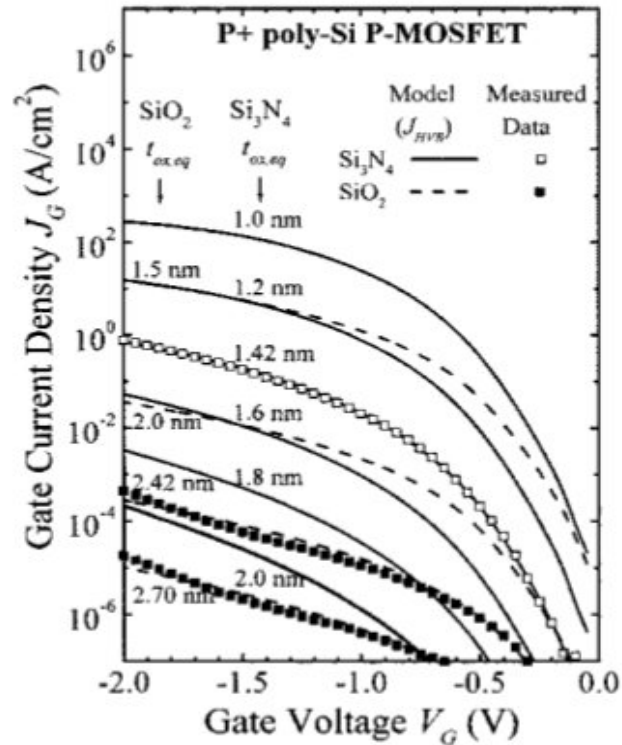
Existing 90nm Process
Capacitance = 1x
Leakage Current = 1x



A potential high- process
Capacitance = 1.6x
Leakage Current = 0.01x

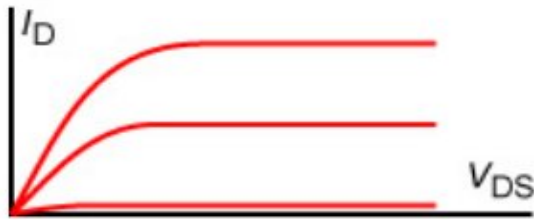
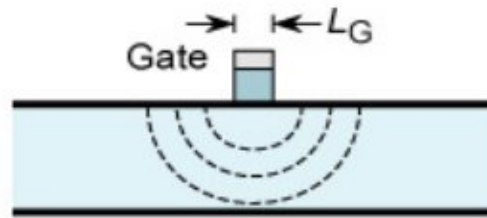
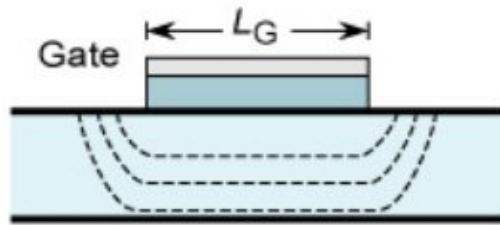
Quantum tunneling

➤ Oxides < 1.2nm



Even for a perfect oxide there is a lower thickness limit

To keep gate operation



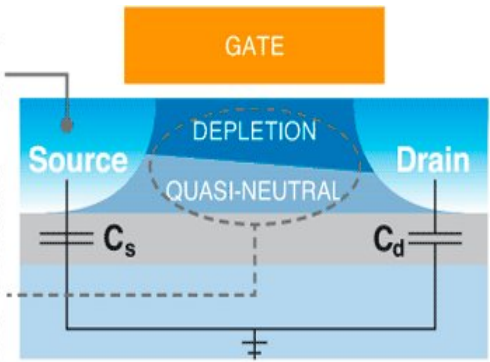
*S*ilicon
*O*n
*I*nsulator

Short channel:

- Current I_{OFF}
- Threshold voltage effect
- Incomplete saturation

The top silicon layer is typically between 50 and 90 nm thick, depending on the design

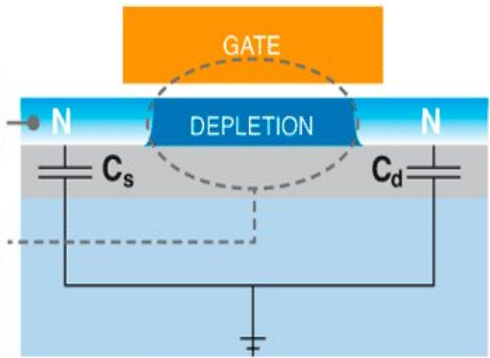
Silicon under the channel is partially depleted of mobile charge carriers. Avalanche ionization at the drain can lead to charges accumulating in the quasi-neutral region ("floating body effect")



Partially depleted SOI MOS transistor cross-section

The top silicon layer is between 5 and 20nm thick, typically 1/4 of the gate length

Silicon under the gate is so thin that it is fully depleted of mobile charges. There is no floating body effect.



Fully depleted SOI MOS transistor cross-section