Φ – 575 Διάλεξη 13

Φυσική διατάξεων δισδιάστατων ημιαγωγών

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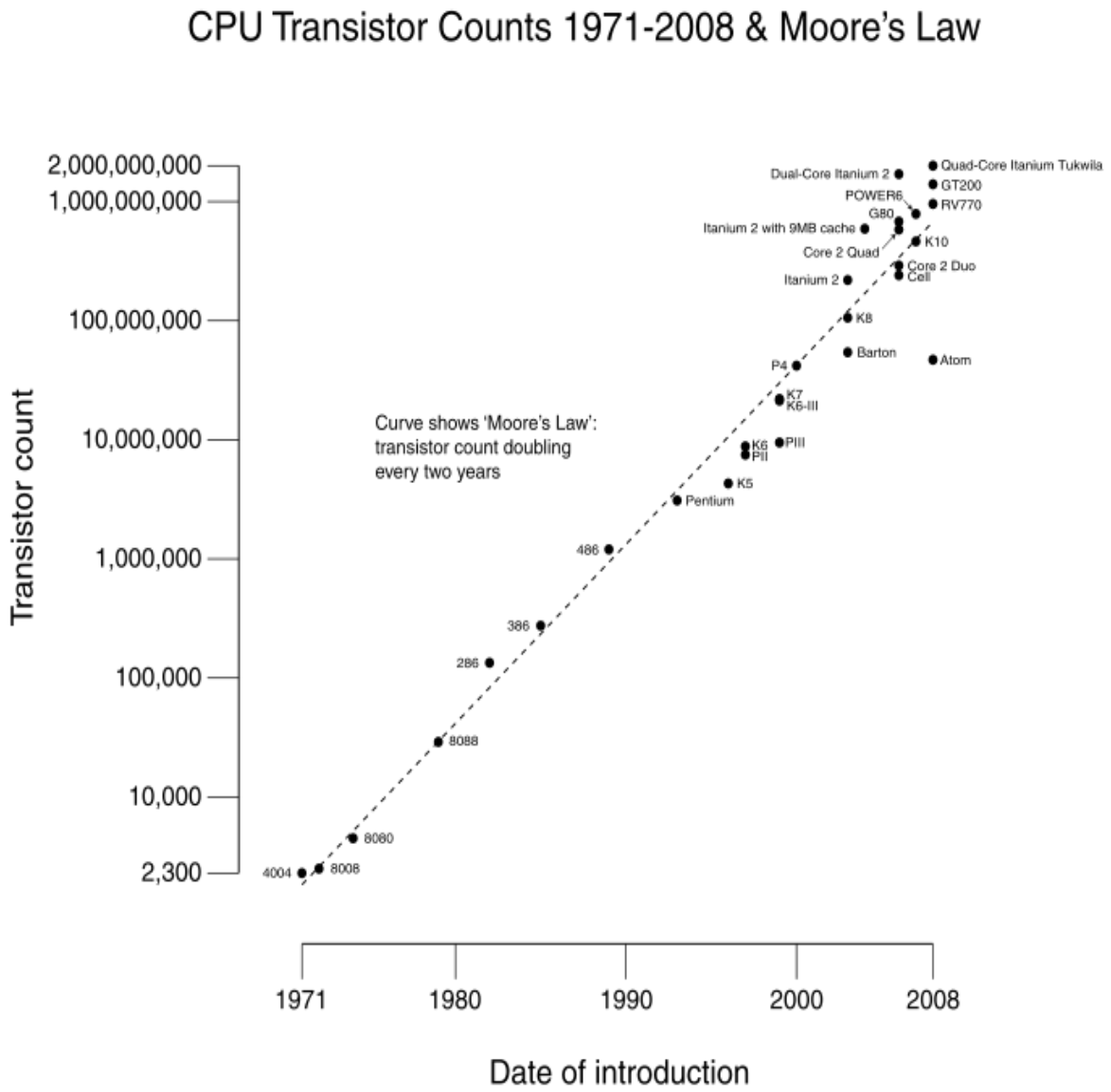
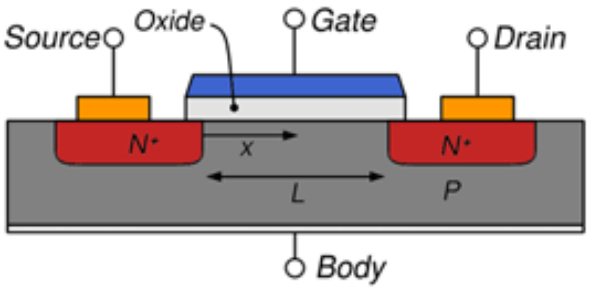
Complexity – Moore's Law

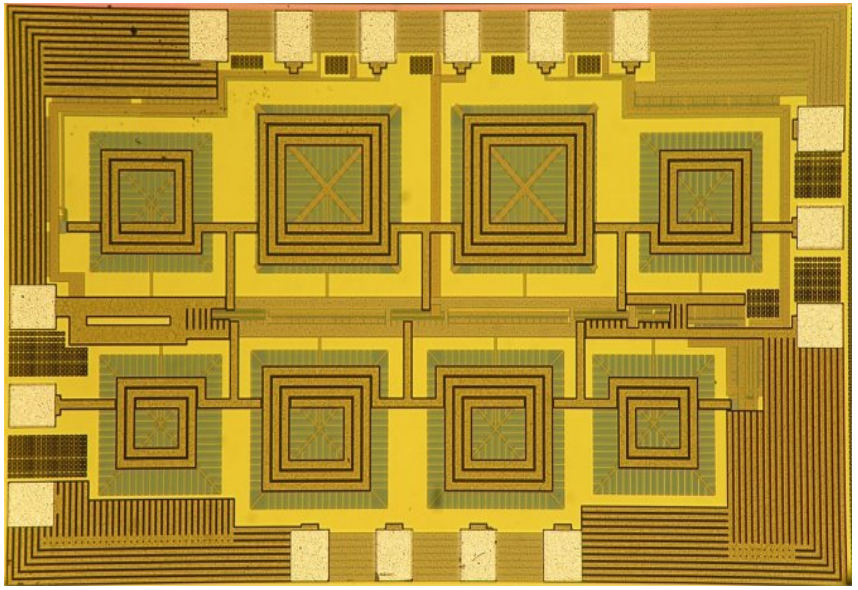
Transistor number:

- *Radical increase*
- *Complex functions*
- *High operating speed*
- *Reduced consumption*



Building blocks





Building blocks:

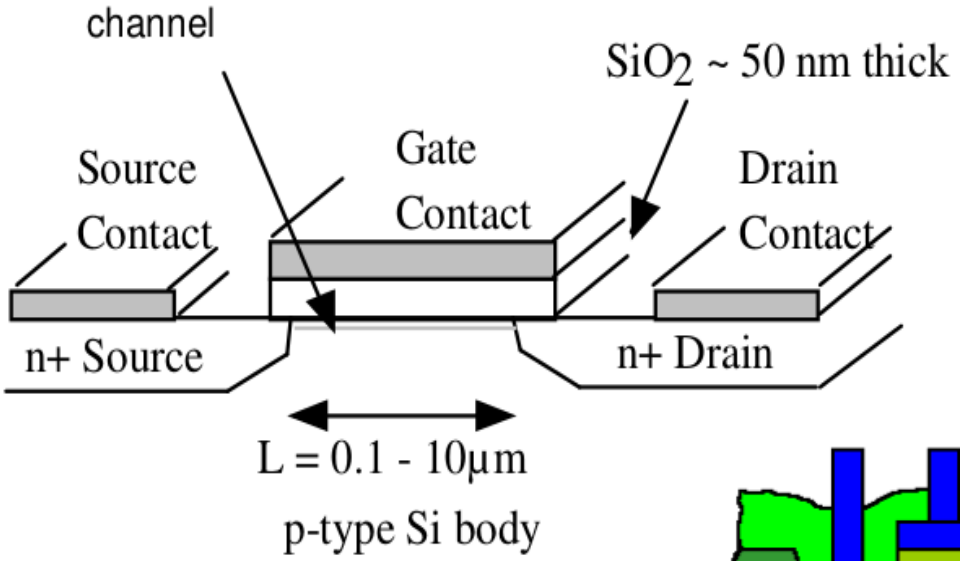
- *Capacitors*
- *Inductances*
- *Resistances*
- *Transistors*
- *Wires*

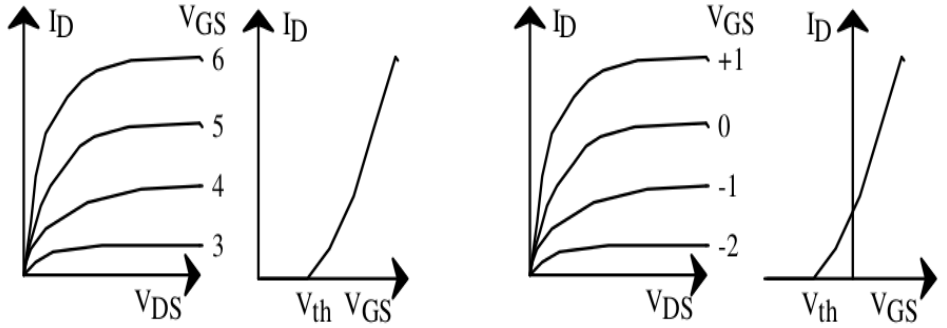
Fabrication on a flat surface with reduced size

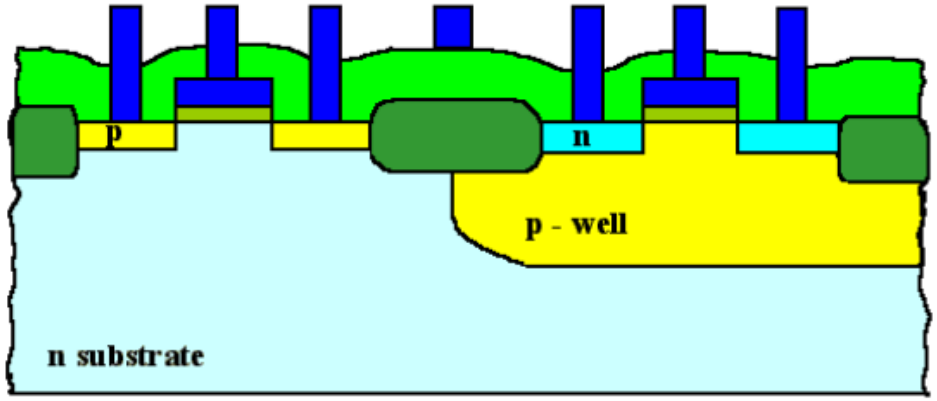
Silicon MOSFET

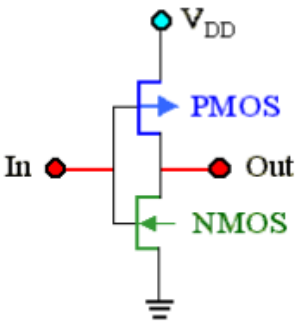
MOSFET:

- *Easy construction (planar)*
- *Small size*
- *Complementary MOS (CMOS)*
- *The basis of contemporary electronics*

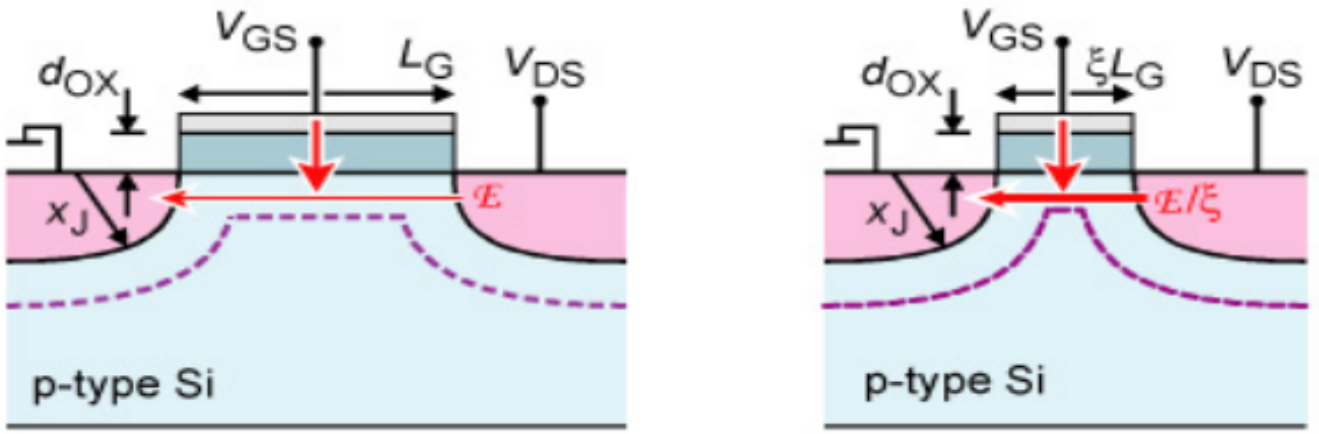








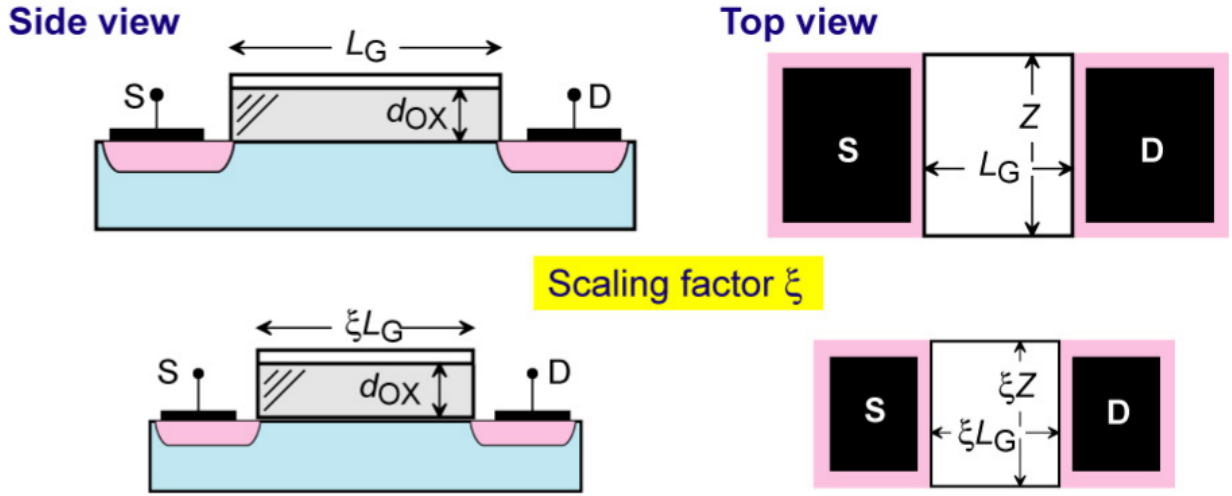
Size



Size reduction:

- *Small footprint thus dense circuits*
- *Small transit time thus faster*
- *Small gate thus reduced paracitic capacitance*
- *Reduced operating voltage thus reduced consumption*

Size

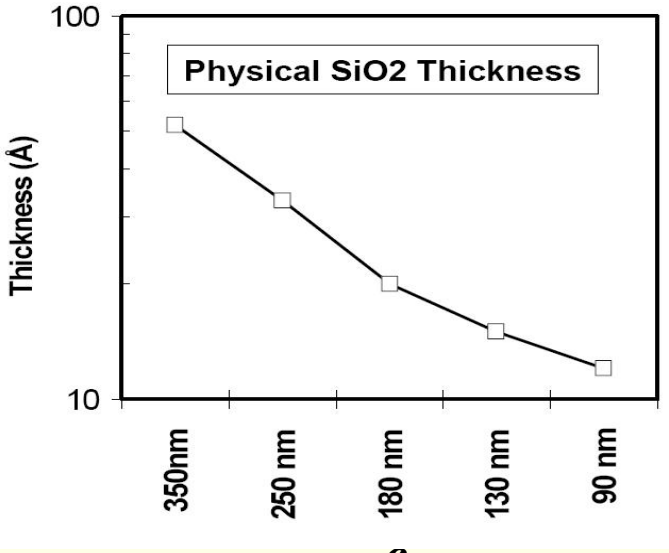


Downscaling by a factor of ξ:

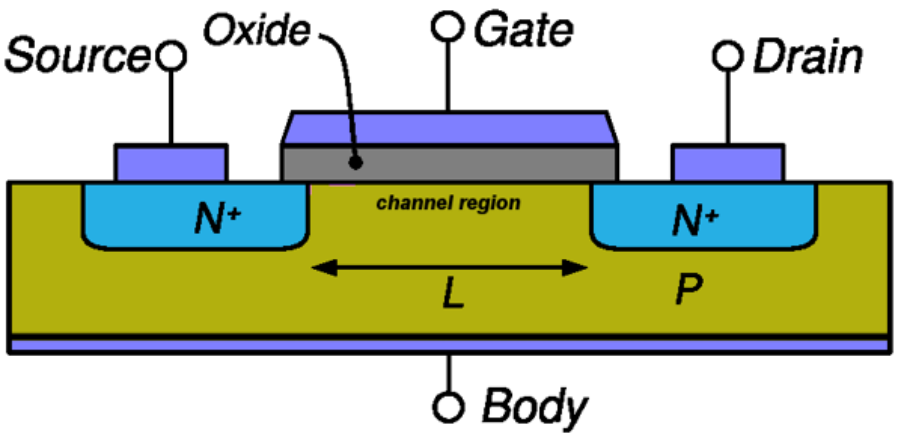
- *Size reduction ξ^2*
- *Gate capacitance $1/\xi^2$*
- *Oprating voltage $1/\xi$*
- *Speed ~ξ*
- *Threshold voltage UNCHANGED*
- *Heat density ???*

To keep the threshold voltage

- *Thinner gate oxide*
- *Increase in doping density*



Transistors 101



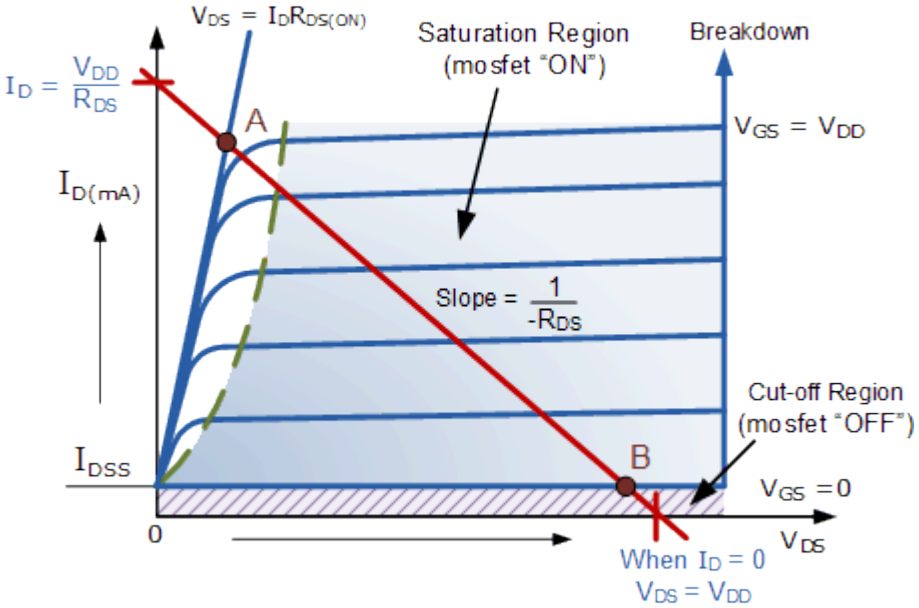
Speed parameters:

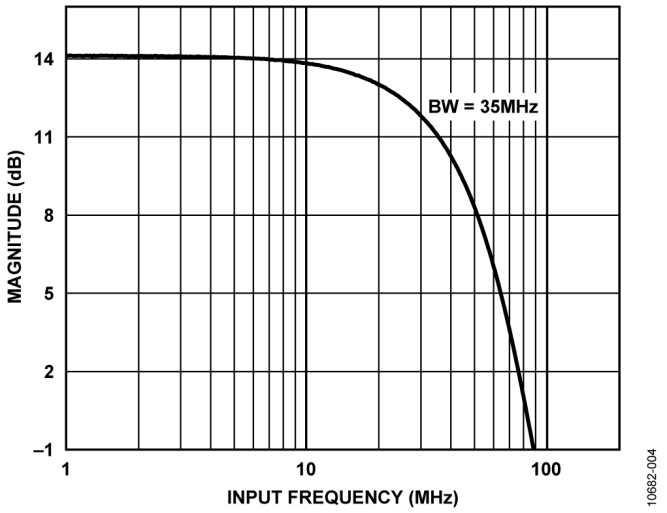
- Carrier velocity

  $2\times10^{7}\ cm/s$
- Channel length

Current control:

- Bandgap
- Access resistance
- Gate – Oxide – Channel capacitor





Replacing oxides

Instead of reducing the thickness we increase ε

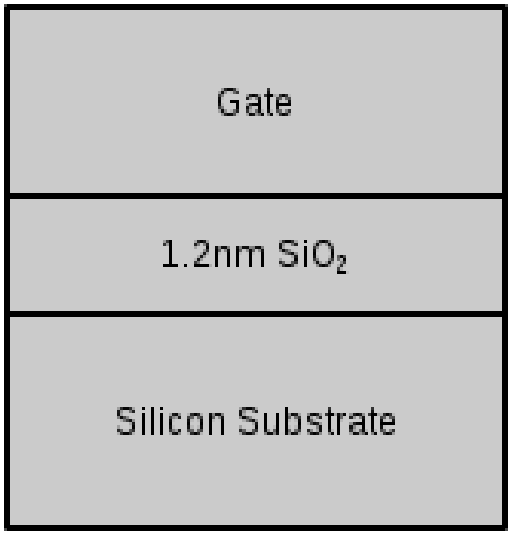
$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{d}$$

Instead of SiO2 ε = 3.9

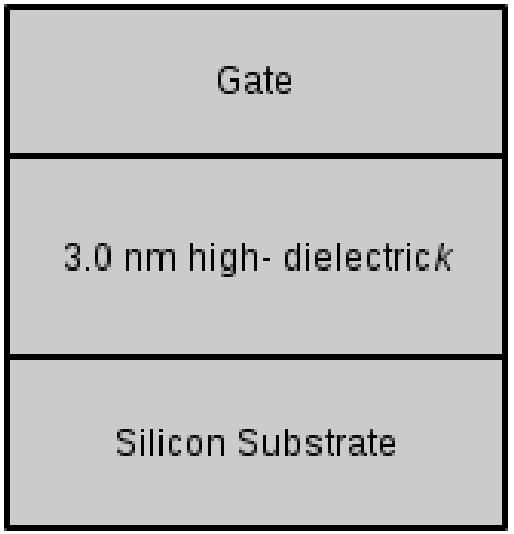
We now use:

HfO ε= 25

ZrO_2 ε= 22



Existing 90nm Process
Capacitance = 1x
Leakage Current = 1x

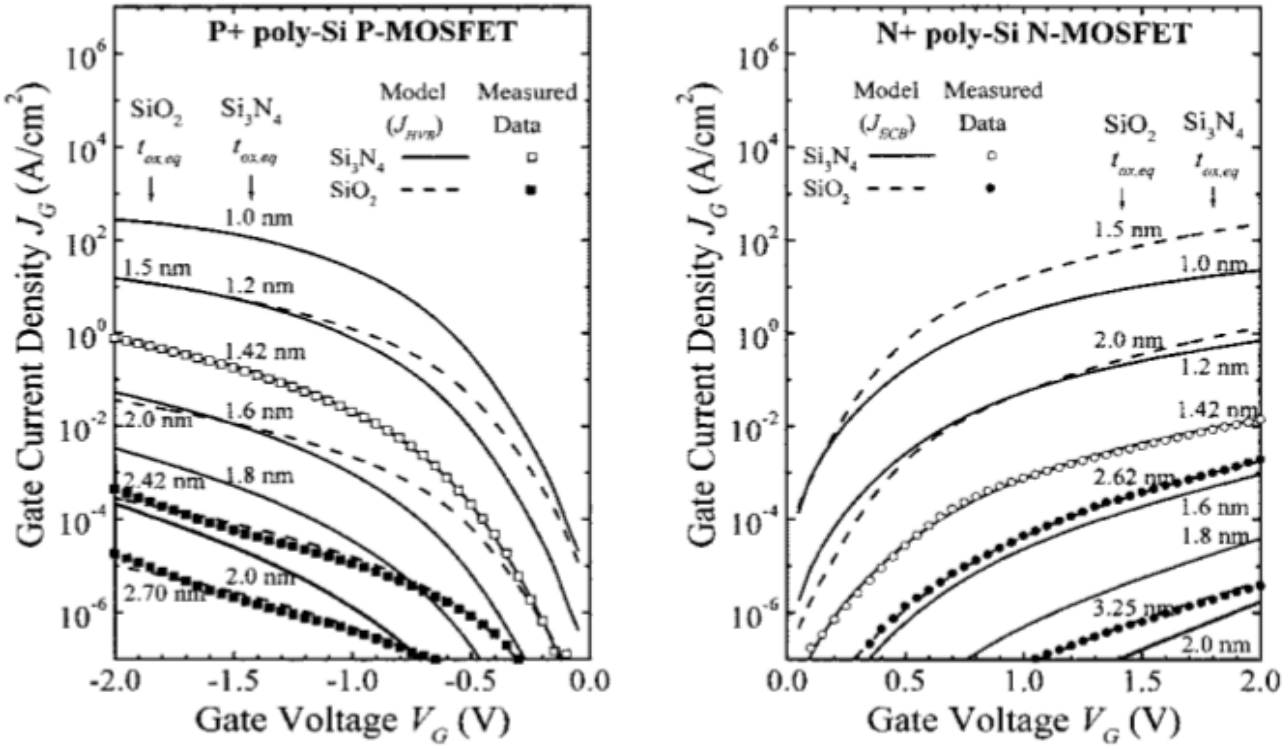


A potential high- process*k*
Capacitance = 1.6x
Leakage Current = 0.01x

Current leakage

Quantum tunneling

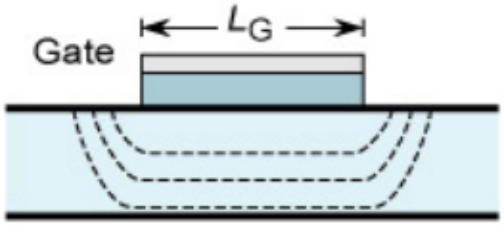
- *Oxides < 1.2nm*

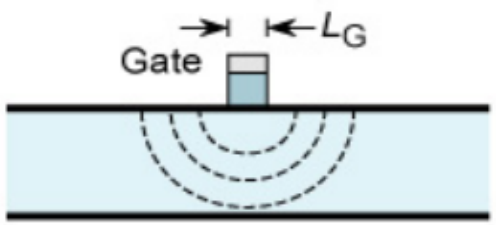


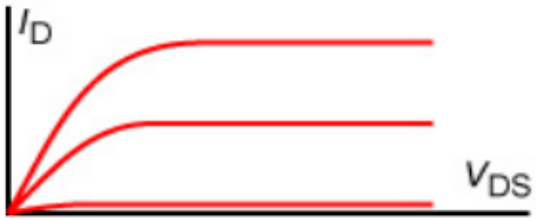
Even for a parfect oxide there is a lower thickness limit

To keep gate operation

Short channel problems







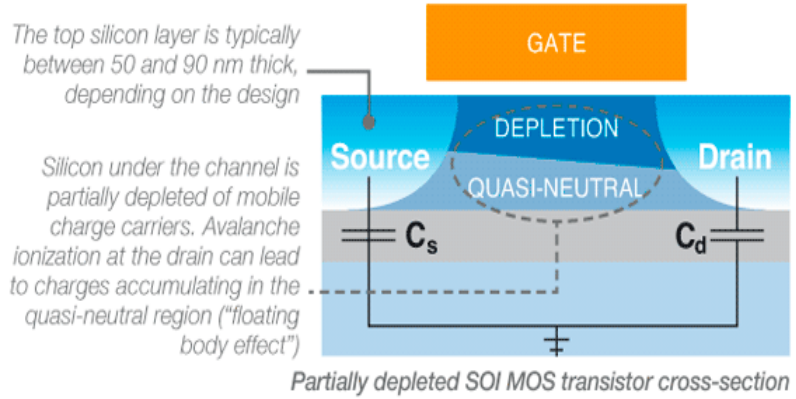
S *ilicon*

O *n*

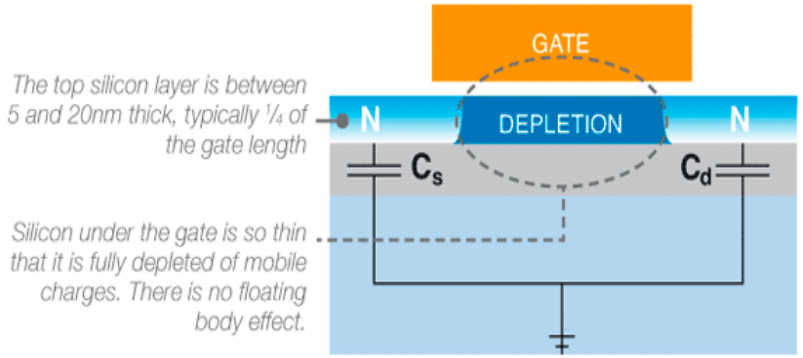
I *nsulator*

Short channel:

- *Current* I_{OFF}
- *Threshold voltage effect*
- *Incomplete saturation*



Partially depleted SOI MOS transistor cross-section



Fully depleted SOI MOS transistor cross-section